IFW

CERTIFICATE OF MAILING BY "FIRST CLASS MAIL"
UNDER 37 CFR 1.8 - SEPARATE PAPER

DOCKET NO.: NPO-20535-2-CU

In Re Application of: Adrian Stoica, et al.

Serial Number: 10/768,754 Filed: January 26, 2004

For: EVOLUTIONARY TECHNIQUE FOR AUTOMATED SYNTHESIS OF ELECTRONIC CIRCUITS

Group Art Unit Unknown Examiner Unknown

I hereby certify that this paper and every paper referred to therein as being enclosed is deposited with the United States Postal Service as " First Class Mail" under 37 CFR 1.8 on the date indicated below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

I hereby certify that the following were placed in the envelope by me and are enclosed herewith for filing:

[X] Information Disclosure Statement (1 Page) with PTO Form 1449 (2 Pages) and 15 non-patent literature documents

[X] Return Postcard (1)

" First Class Mail"
Date of Deposit: May 19, 2004

John H. Kusmiss

John H. Kusmiss, 32,149
818-354-7770

Patent

NASA Case No. NPO-20535-2-CU

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Adrian Stoica, et al.	)	Examiner: Unknown
Entitled: EVOLUTIONARY TECHNIQUE FOR AUTOMATED SYNTHESIS OF ELECTRONIC CIRCUITS	)	Group Art Unit: Unknown
Serial No.: 10/768,754	)	
Filing Date: January 26, 2004	)	

INFORMATION DISCLOSURE STATEMENT

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby cites patent and/or publications for consideration by the Patent and Trademark Office in regard to the claimed invention on the attached form. By this notice the applicant requests that the Patent and Trademark Office make of record the documents listed. No representation is made that more pertinent material is not available or should not be considered by the Examiner. It is expected that the Patent and Trademark Office will independently conduct a complete search of appropriate art. Furthermore, no admission is being made that these documents are prior art, and applicant reserves the right to challenge any such consideration.

Respectfully submitted,

Dated May 19, 2004

John H. Kusmiss

John H. Kusmiss
Attorney of Record 32,149
(818) 354-7770

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Sheet 1 of 2	Application Number: 10/768,754 Filing Date: January 26, 2004 First Named Inventor: Adrian STOICA, et al. Group Art Unit: Unknown Examiner Name: Unknown Attorney Docket Number: NPO-20535-2-CU

Examiner Initials	NON PATENT LITERATURE DOCUMENTS
	BENNETT, F. III, et al. "Evolution of a 60 decibel Op Amp Using Genetic Programming", *First Int'l. Conf. On Evolvable Systems*, Springer-Verlag, Japan, 1996, pp. 455-469.
	FLOCKTON, STUART J., et al., "Intrinsic Circuit Evolution Using Programmable Analogue Arrays," *Proc. Of the Second Int'l. Conf. On Evolvable Systems: From Biology to Hardware*, Springer-Verlag, Switzerland, 1998, pp. 144-153.
	IBA, HITISHI, et al., "Machine Learning Approach to Gate-Level Evolvable Hardware," *Proc. Of the First Int'l. Conf. On Evolvable Systems*, Springer-Verlag, Japan, 1996, pp. 327-343.
	KAJITANI, ISAMU, et al., "A gate-level Ettw Chip: Implementing GA operations and reconfigurable hardware on a single LSI," *Proc. Of the Second Int'l. Conf. On Evolvable Sytems: From Biology to Hardware*, Springer-Verlag, Berlin, 1998, pp. 1-12.
	KOZA, JOHN R., et al., "Reuse, Parameterized Reuse, and Hierarchical Reuse of Substructures in Evolving Electrical Circuits Using Genetic Programming," *Proc. Of the First Int'l. Conf. On Evolvable Systems*, Springer-Verlag, Japan, 1996, pp. 312-326.
	KOZA, JOHN R., et al., "Automated WYWIWYG Design of Both the Topology and Component Values of Electrical Circutis Using Genetic Programming," *Proc. Of the First Annual Genetic Programming Conference*, MIT Press, Cambridge MA, 1996, pp. 123-131.
	KOZA, JOHN R. et al., "Automated Synthesis of Analog Electrical Circuits by Means of Genetic Programming," *IEEE Transaction on Evolutionary Computation*, Vol. 1, No. 2, 1997, pp. 109-128.
	LOHN, JASON D., et al., "Automated Analog Circuit Synthesis Using a Linear Representation," *Proc. Of the Second Int'l. Conf. On Evolvable Systems: From Biology to Hardware*, Springer-Verlag, Berlin, 1998, pp. 125-133.
	MURAKAWA, MASAHIRO, et al., "Analogue EHW Chip for Intermediate Frequency Filters," *Proc. Of the Second Int'l. Conf. On Evolvable Systems: From Biology to Hardware*, Springer-Verlag, Berlin, 1998, pp. 143-143.
	STOICA, ADRIAN, "On Hardware Evolvability and Levels of Granularity," *International Conference On Intelligent Systems and Semiotics*, NIST, Gaithersburg VA, September 1997, pp. 244-247.
	THOMPSON, ADRIAN, "Silicon Evolution," *Proc. Of the First Annual Genetic Programming Conference*, MIT Press, Cambridge MA, 1996, pp. 444-452.
	THOMPSON, ADRIAN, "On the Automatic Design of Robust Electronics Through Artificial Evolution," *Proc. Of the Second Int'l. Conf. On Evolvable Systems: From Biology to Hardware*, Springer-Verlag, Switzerland, 1998, pp. 13-24.
	THOMPSON, ADRIAN, "An evolved circuit, intrinsic in silicon, entwined with physics," *Proc. Of the First Int'l. Conf. On Evolvable Systems*, Springer-Verlag, Japan, 1996, pp. 390-405.

Examiner's Signature:	Date Considered:

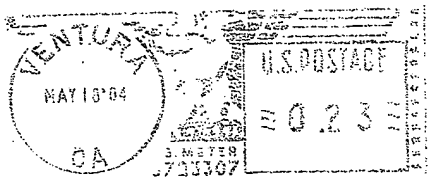
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Sheet 2 of 2	Application Number: 10/768,754 Filing Date: January 26, 2004 First Named Inventor: Adrian STOICA, et al. Group Art Unit: Unknown Examiner Name: Unknown Attorney Docket Number: NPO-20535-2-CU

Examiner Initials	NON PATENT LITERATURE DOCUMENTS
	ZEBULUM, RICHARD S., et al., "Evolvable Systems in Hardware Design: Taxonomy, Survey and Applications," *Proc. Of the First Int'l. Conf. On Evolvable Systems*, Springer-Verlag, Japan, 1996, pp. 344-358.
	ZEBULUM, RICHARD S., et al., "Analog Circuits Evolution in Extrinsic and Intrinsic Modes," *Proc. Of the Second Int'l. Conf. On Evolvable Systems: From Biology to Hardware*, Springer-Verlag, Berlin, 1998, pp. 154-165.

Examiner's Signature:	Date Considered:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



John H. Kusmiss
NASA Management Office - JPL
4800 Oak Grove Drive, M/S 180-200
Pasadena, CA 91109-8099

NASA CASE NO.	: NPO-20535-2-CU
FILING DATE	: 10/768,754
APPLICATION SERIAL NO.	: January 26, 2004
APPLICANT	: Adrian Stoica, et al.
TITLE:	: EVOLUTIONARY TECHNIQUE FOR AUTOMATED SYNTHESIS OF ELECTRONIC CIRCUITS

RECEIPT OF THE FOLLOWING PAPERS IS EVIDENCED HEREON BY THE OFFICIAL STAMP OF THE UNTIED STATES PATENT AND TRADEMARK OFFICE.

INFORMATION DISCLOSURE STATEMENT 1 Page, w/PTO Form 1449
2 Pages w/15 non-patent literature documents

5-19-04